In the Claims:

1. (Canceled)

2. (Currently Amended) The method according to Claim [[1]] 28, further comprising chemically-mechanically polishing the surface of the wafer to remove the first conductive layer, second conductive material, thin dielectric layer, and third conductive material from the top surface of the insulating layer, leaving at least one vertical MIMCap in the insulating layer first region.

3. (Original) The method according to Claim 2, wherein a plurality of vertical MIMCap's are formed in the insulating layer first region, further comprising coupling at least two of the vertical MIMCap's together.

4. (Original) The method according to Claim 2, wherein the CMP simultaneously forms MIMCap's in the insulating material first region and conductive wiring in the insulating material second region.

5. (Currently Amended) The method according to Claim [[1]] 28, wherein depositing the first conductive layer comprises depositing a conductive liner.

6. (Original) The method according to Claim 5, wherein depositing the first conductive layer comprises forming a conductive seed layer over the conductive liner.

7. (Original) The method according to Claim 6, wherein the conductive liner and conductive seed layer comprise at least one MIMCap bottom plate.

8. (Original) The method according to Claim 6, wherein depositing the conductive liner comprises depositing TaN, Ta, TiN or combinations thereof by chemical vapor deposition (CVD) or physical conductive vapor deposition (PVD), wherein forming the conductive seed layer comprises depositing a copper seed layer by PVD or CVD.

9. (Currently Amended) The method according to Claim [[1]] 28, wherein depositing the second conductive layer comprises depositing copper by electroplating or physical vapor deposition (PVD), wherein depositing the third conductive material comprises depositing W, TiN, Al, Ta, Ti, TaN, TiW, Cu, Si, or combinations thereof by physical vapor deposition (PVD) or chemical vapor deposition (CVD), wherein the third conductive material forms the MIMCap top plate.

10. (Currently Amended) The method according to Claim [[1]] 28, wherein depositing the thin dielectric layer comprises depositing a conformal dielectric having a thickness of 10 nm to 200 nm.

11. (Original) The method according to Claim 10, wherein depositing the thin dielectric layer comprises depositing silicon nitride, Ta_2O_5, or combinations thereof by plasma-enhanced chemical vapor deposition (PECVD).

12. (Currently amended) A method of fabricating a vertical metal-insulator-metal capacitor (MIMCap), comprising:

providing a ~~wafer having a~~ workpiece;

depositing an inter-level dielectric over the workpiece;

patterning the inter-level dielectric ~~with~~ to form a plurality of trenches, said inter-level dielectric comprising at least one first region and at least one second region, the first region comprising trenches for at least one MIMCap, the second region comprising trenches for a plurality of conductive lines, wherein the trenches in the first region and the trenches in the second region have substantially vertical sidewalls and equal height and width dimensions;

depositing a conductive liner over the inter-level dielectric within the trenches;

depositing a seed layer over the conductive liner;

depositing a resist over the seed layer;

removing the resist over the seed layer in the inter-level dielectric second regions, leaving resist over the seed layer in the inter-level dielectric first regions;

depositing a first conductive material within the inter-level dielectric second region trenches to form a plurality of conductive lines;

removing the resist;

depositing a MIMCap dielectric over the first conductive material within the second region trenches and over the first conductive layer within the first region trenches; and

depositing a second conductive material over the MIMCap dielectric within the first region trenches to form a MIMCap top plate, wherein the second conductive material completely fills the first region trenches.

13. (Original) The method according to Claim 12, further comprising chemically-mechanically polishing (CMP) the top surface of the wafer to remove the conductive liner, seed layer, first conductive material, MIMCap dielectric, and second conductive material from the top surface of the inter-level dielectric, leaving at least one vertical MIMCap in the insulating layer first region.

14. (Original) The method according to Claim 13, wherein a plurality of vertical MIMCap's are formed in the inter-level dielectric first region, further comprising coupling at least two of the vertical MIMCap's together.

15. (Original) The method according to Claim 13, wherein the CMP simultaneously forms at least one MIMCap in the inter-level dielectric first region and the plurality of conductive lines in the inter-level dielectric second region.

16. (Original) The method according to Claim 12, wherein the conductive liner and conductive seed layer comprise at least one MIMCap bottom plate.

17. (Original) The method according to Claim 12, wherein depositing the conductive liner comprises depositing TaN, Ta, TiN or combinations thereof by chemical vapor deposition (CVD) or physical conductive vapor deposition (PVD), wherein forming the conductive seed layer comprises depositing a copper seed layer by PVD or CVD.

18. (Original) The method according to Claim 12, wherein depositing the first conductive layer comprises depositing copper by electroplating or physical vapor deposition (PVD), wherein depositing the second conductive material comprises depositing W, TiN, Al, Ta, Ti, TaN, TiW, Cu, Si, or combinations thereof by physical vapor deposition (PVD) or chemical vapor deposition (CVD).

19. (Original) The method according to Claim 12, wherein depositing the MIMCap dielectric comprises depositing a conformal dielectric having a thickness of approximately 10 nm to 200 nm.

20. (Original) The method according to Claim 19, wherein depositing the MIMCap dielectric comprises depositing silicon nitride, Ta_2O_5, or combinations thereof by plasma-enhanced chemical vapor deposition (PECVD).

21. (Currently Amended) A method of fabricating a vertical metal-insulator-metal capacitor (MIMCap), the method comprising:

forming a first trench and a second trench in an insulating layer, the first trench and second trench having substantially vertical sidewalls and substantially equal height and width dimensions;

forming a first conductive layer lining the first and second trenches;

forming a dielectric layer over the first conductive layer in the first trench but not in the second trench; and

forming a second conductive layer over the dielectric layer in the first trench and over the first conductive layer in the second trench, such that the second conductive layer substantially fills both the first trench and the second trench.

22. (Previously Presented) The method according to Claim 21, further comprising masking the second trench prior to forming the dielectric layer.

23. (Previously Presented) The method according to Claim 21, wherein the insulating layer comprises a top surface, further comprising chemically-mechanically polishing the insulating layer to remove the first conductive layer, second conductive layer, and dielectric layer from the top surface of the insulating layer, leaving a vertical MIMCap in the first trench.

24. (Currently Amended) The method according to Claim 23, wherein forming the first trench comprises forming a plurality of first trenches in the insulating layer, wherein chemically-mechanically polishing the insulating layer comprises forming a plurality of vertical MIMCaps

~~MIMCap's~~ in the plurality of first trenches, further comprising coupling at least two of the vertical MIMCaps ~~MIMCap's~~ together.

25. (Currently Amended) The method according to Claim 23, wherein chemically-mechanically polishing the insulating layer simultaneously forms ~~MIMCap's~~ a MIMCap in the first trench and conductive wiring in the second trench.

26. (Previously Presented) The method according to Claim 21, wherein depositing the first conductive layer comprises depositing a conductive liner over the insulating layer and forming a conductive seed layer over the conductive liner.

27. (Previously Presented) The method according to Claim 26, wherein the conductive liner and conductive seed layer comprise a MIMCap bottom plate.

28. (New) A method of fabricating a metal-insulator-metal capacitor (MIMCap), comprising:

depositing an insulating layer over a workpiece, the insulating layer including a MIMCap region and wiring region;

patterning the insulating layer to form a plurality of trenches, each trench including substantially vertical sidewalls and each trench in the MIMCap region having substantially equal height and width dimensions as each trench in the wiring region;

depositing a first conductive layer over the insulating layer and within the trenches in both the MIMCap region and the wiring region;

depositing a resist over the MIMCap region of the insulating layer;

depositing a second conductive material within the trenches in the wiring region of the insulating layer;

removing the resist;

depositing a thin dielectric layer over the second conductive material within the wiring region trenches and over the first conductive layer within the MIMCap region trenches; and

depositing a third conductive material over the thin dielectric layer within the MIMCap region trenches to completely fill the MIMCap region trenches.